Report from the Silicon Upgrade Task Force

Marcel Demarteau, Brenna Flaugher, Joe Incandela, Ron Lipton, Petros Rapidis, Jeff Spalding, William Wester

June 17, 2001

Introduction

The PAC recommended at their last meeting that a task force be setup to study the commonality between the silicon detectors proposed for the two collider detectors, CDF and DØ, for Run 2b. On May 4, 2001 the Fermilab directorate asked Marcel Demarteau (co-chair), Brenna Flaugher(co-chair), Joe Incandela, Ron Lipton, Petros Rapidis, Jeff Spalding, William Wester to participate in this task force. The charge to the committee was:

> "The success of the Run IIb upgrades for CDF and D0 will be crucial for the future high luminosity collider program. Since there is little time to accomplish these upgrades and always pressure on funding, the Lab would like to take advantage of common designs for the two detectors. The Silicon Upgrade Task Force is being set up to review the designs of the CDF and D0 Run IIb silicon detector designs and to recommend common solutions to common problems wherever appropriate. (A separate cost review of the Run IIb upgrades is also being undertaken by PPD with some overlap with the task force.) It is expected that other experts associated with the silicon upgrade will be asked to participate in the various discussions of the Task Force.
>
> The Task Force should also make suggestions for common design studies that should be undertaken and comment on priority R&D efforts that should be started early. To meet the Run IIb schedule, it may be necessary to exercise descoping options; the Task Force should comment on possible areas that would provide these descoping options.
>
> The Task Force should prepare a written report of these deliberations to be submitted by June 14 and presented to the Fermilab PAC at the Aspen meeting in June."

Over the course of the last two months the task force met among themselves and with associated experts from the two experiments and SiDet. Some of the experts consulted are Nicola Bacchetta, Bill Cooper, Regina Demina, Jim Fast, Mike Hrycyk, Marvin Johnson, Hans Jostlein, Rich Partridge, Ray Yarema, Sergio Zimmermann and Tom Zimmerman. The meetings were aimed at probing the two experiments, trying to uncover aspects common between them. Both experiments, however, work within their boundary conditions, which are set by the geometry of the detector and the performance of the surrounding detectors in which the silicon trackers are embedded. This report will first

describe these boundary conditions and how they affect key aspects of the designs of the Run2b silicon detectors. Common areas between the two detectors are then described, followed by the recommendations of the task force. It should be emphasized here that both experiments have found these discussions very helpful and have expressed a desire that these discussions continue on a regular basis.

Experimental Boundary Conditions

For CDF the primary boundary conditions and their implications are:

- CDF will retain the ISL and thus has two silicon layers at radii of approximately R=210 and 290mm, respectively. The ISL and the outermost three layers of the SVXIIb are designed to perform the tracking. The innermost layers can be designed to aid in the tagging efficiency.
- The new silicon detector has to fit within the ISL with an inner radius of 180mm
- The COT has full coverage up to |eta|<1.0, with rapidly decreasing acceptance beyond |eta|<1.0. The limited coverage of the COT demands that the silicon system provide stand-alone tracking in the region 1.0 < |eta| < 2.0, and drives the design towards longer coverage in z.

The CDF design strategy is to do pattern recognition in the outer three layers and the ISL. Each outer layer of the Run2b detector has an axial sublayer and a small angle stereo sublayer. These five layers have a lever arm of 20cm and an expected pointing resolution in z of 350-700? m. For the innermost layers 90-degree stereo readout is being considered. The intent is to use the z information in the inner layers to improve the resolution in z after the track is found, without degrading the impact parameter resolution. This would provide the possibility for 3d vertex reconstruction and improve the rejection for mistags, notably for the two-track tags. CDF is planning to use fine pitch high density cables to connect the sensors to the hybrids. This scheme of off-board electronics removes significant mass from the tracking volume (the hybrids + associated cooling) and allows passive cooing of the silicon sensors.

For DØ the key characteristics are:

- The overall length of the new silcon detector is constrained to a maximum length of 1320mm for the tracker to be installed in the collision hall. This in turn requires that on-board electronics (as opposed to removing electronics with low mass cables) be used.
- The new silicon detector has to fit within the scintillating fiber tracker with an inner radius of 180mm.
- The scintillating fiber tracker has full coverage up to |eta|<1.6. To maximize the potential of the fiber tracker, the acceptance of the silicon detector needs to be matched with the fiber tracker. In addition DØ plans stand-alone silicon tracking in the region 1.6 < |eta| < 2.0 to extend their tracking coverage to match the region where they have good lepton identification.

DØ requires six axial and at least four small angle stereo layers for pattern recognition and impact parameter measurement. The constraint on the overall length of the modules for the outer layers forces a design, which has on-board electronics, i.e. hybrids mounted on the silicon modules. This in turn determines that the CDF and DØ cooling on the outer layers will be quite different. On-board electronics will require a large cooling capacity internal to the tracker modules, while the module cooling needs for the off-board design are significantly less.

Although the experiments will differ in their details, there are many common features. A common approach and use of common technology can lead to great benefits. Observations on common areas are discussed below.

Luminous Region

The accelerator division (M. Church) has provided the task force the current understanding of the weekly integrated luminosity as function of the fiducial length. Both experiments are using this information to determine the base length of their silicon tracker.

Beampipe

Both CDF and DØ are hoping to use a drilled beampipe. The maximum length quoted for a 1" diameter pipe is 0.8m with a wall thickness of 0.5mm. Wall thickness increases linearly with length; a 1.1m long drilled beampipe would have a wall thickness of 0.8mm. Currently both experiments are considering different length and different radius beampipes, driven by the overall geometry of the detector. CDF is contemplating a slightly larger diameter beampipe than the current Run 2a design. If the designs were the same Electrofusion, the only reliable vendor for beampipes, quotes a 32 week delivery for a drilled beam pipe with a second pipe delivery 10 weeks later. It is recommended that the projects pursue a joint purchase when the designs settle down. Given the long lead times, the joint purchase order should be submitted as quickly as possible

Support Structures

Inner Layers

There is a large area of commonality between the two projects for the inner layers. Both projects will have carbon-fiber structures surrounding the beampipe for the innermost layers. Both projects will have off-board electronics for the inner layers. These structures are hard to build. They require high precision, integrated cooling, high thermal conductivity, high stiffness, to name just a few of the qualifications. Because of this an extensive R&D period is required to qualify the structures and should commence immediately. Building of the production devices is anticipated to take a long time. Moreover, multiple structures will be needed for the two projects.

Outer Layers

For the outer layers there is a natural branching point given that CDF intends to have off-board electronics, whereas DØ, due to space constraints, is forced to on-board electronics. There are still many similarities in their conceptual design. For the outer layers both experiments are considering carbon-fiber support structures. The staves, mounted on the support cylinders, will have modules on either side. The alignment of these staves and the rigidity of the support cylinders will be provided by precision flanges in the middle and at the end of the cylinders. The projects will diverge with respect to the cooling. DØ will require active cooling, since they have to cool both the hybrids and the silicon. CDF will only need passive cooling for the silicon in the outer layers.

Recommendation:

R&D effort on support structures and prototyping should commence as quickly as possible and funds have to be provided. Learning experiences and exchange of ideas should take place regularly in a well defined forum.

Flex Cables

Both projects need high density fine pitch flex cables for their inner detectors. Since CDF is considering employing only off-board electronics, flex cables are needed for the whole tracker. The cables would be similar to the cables made by CERN for the layer00 project. Because a large number of these cables are needed, and since they are technically very challenging, they constitute a high cost and schedule risk. CDF is in contact with Keycom in Japan and DØ is in contact with Dyconex in Zurich. It is recommended that both experiments work together on qualifying vendors and exchange experiences.

Hybrids

Two technologies are being considered for hybrids: flexible circuits laminated to Be, or ceramic hybrids. CDF has experience with ceramic hybrids and intends to use them for all layers. DØ has experience with laminated flex circuits and intends to use them for the outer layers. For the inner layers ceramic hybrids are being considered. The experiments should base their choice on their previous experience. The task force, though, recommends that both projects continue their dialogue.

Cooling

For a $15fb^{-1}$ lifetime and an inner radius of 1.3cm CDF estimated that the silicon needs to be kept at a temperature of -5 degrees C. DØ aims for an operating temperature of the silicon of -10 degrees C. This is on the edge of what a water glycol mixture can provide. Prototyping is warranted. Cooling to the lowest possible temperatures limits leakage currents and thus extends the life of the detector, but there are uncertainties in the estimates. Both CDF and DØ may investigate alternate coolants, especially for the innermost layers.

Recommendation: the projects should, if possible, utilize the existing water glycol systems. To improve performance new fluids can be investigated, that could simply replace the glycol water mixture. The results of these studies should be shared between the projects.

Sensors

At the time of the April PAC meeting CDF was considering three different sensor lengths: 66, 83 and 100mm, whereas DØ was considering two lengths: 80 and 108mm. Masks and details of the sensor layout are likely to be different for each experiment. They do not drive the cost given the large number of sensors that have to be purchased. There is, however, substantial benefit to coordinating procurement and technical specifications.

CDF is considering thin silicon (150 μm) for the inner 90 degree layers. If this is adopted, prototyping is needed. DØ is going to revisit the option of 90 degree stereo layers. Double metal layers are being considered by CDF. Double metal sensors versus ganging in cables depends on cable vendors and difficulty in cable fabrication.

With the perception that it is likely that the experiments will use the same vendors for a substantial fraction of their detector orders and that a joint purchase provides the laboratory with more leverage, it is recommended that the experiments cooperate in vendor contacts, share technical and testing information, and ensure that there are no conflicts in delivery schedules. A joint effort between the projects for the quality assurance of sensors should be seriously considered.

Readout Chip

The requirements for CDF and DØ for a silicon readout chip are different in that CDF requires the ability to readout in a deadtimeless fashion while the DØ silicon DAQ system is not deadtimeless. Despite this difference, DØ has shown that it can operate the SVX3d chip (deadtimeless chip) in SVX2 mode (compatible with the DØ DAQ).

The chip geometry and pad frame requirements are also somewhat different between CDF and DØ. CDF would prefer to bus power, biasing, and to provide bypassing along the long edge of the chip. DØ requires wirebond pads for power, biasing, and bypassing off the backend of the chip. CDF utilizes differential transmission of many of its control and data lines while DØ employs single-ended transmission. Despite these differences, the geometry and pad frame is potentially the same for both experiments as redundant pads both on the long side of the chip and the back end can connect power, biasing, and bypassing. Internal chip logic can be used to set the chip in a mode where outputs are presented as single-ended or differential. The programmability can also be used for tying the FE and BE clocks together as required by DØ. Thus, even with these differences, a SVX4 chip design common to both experiments is feasible.

An exactly identical chip has a number of clear advantages to the laboratory and the overall success of RunIIb for both CDF and DØ.

- There would be no additional design effort to layout, verify, and submit a second version of the chip. This time either would not be used for testing and simulation of the first chip or could cause a delay of the chip submission for two versions.
- There would be only one set of masks with an exactly common chip. If there were two nearly identical chips, there would either be two masks or a single mask with both versions

- Fermilab is prepared to take on the responsibility of wafer scale testing for one version of the SVX4. CDF and DØ input is required in any case for the testing effort. If there are two versions of the chip, it is likely that a second testing facility for wafers should be commissioned.
- A single chip version greatly simplifies handling parts in terms of postproduction processing including dicing, availability of spares, etc. Duplicate efforts would be required if the chips are not exactly identical.

The current status of the project is that LBNL, Padova, and Fermilab are all supplying engineering in the development of SVX4. LBNL has the overall responsibility for assembling the device. It has designed a preamp, and is working with Padova on the backend (FIFO, ADC, I/O, etc). Fermilab has responsibility for the pipeline and has also developed a preamp. Both CDF and DØ have contributed to a nearly final set of required specifications.

LBNL submitted a test chip preamp at the end of last year and has performed tests and measurements on the device. It shows the feasibility of the chip in 0.25 micron technology. Fermilab has recently submitted a combination preamp and pipeline test chip. Both a modified LBNL preamp design and the FNAL preamp design will be incorporated with the pipeline design.

A review at LBNL of the SVX4 chip was conducted in April 2001. The overriding conclusion was that steps should be taken so that the first full size chip is likely to be fully functional and as close as possible to the final design. The committee also recommended to test critical circuit blocks through test chip submission to reduce risk in the final submission.

LBNL is beginning the process of integration where all the designed functions get incorporated into the first full size prototype chip. They are also finishing their design and layout of the backend. In assembling the first full-size prototype, the current plan is that two versions will be assembled. In the CDF version, power, biasing, and bypass busing to the backside will not be connected. This also implies that some internal voltages will not be internally connected so that the bypassing and tying of voltages together can be done externally. In the DØ version, internal voltages will be connected and the power, biasing, and bypassing will be bused to the back end. It is an open issue as to whether the pipeline design employed in each version will or will not have internal bypassing as designed by FNAL. It is also an open issue as to whether the Fermilab or LBNL preamp will be employed. The current schedule has the first full-size production chip being submitted in Sept 2001.

There is a perceived technical risk associated with busing power, biasing, and bypassing to the backend as is done for DØ for use by CDF. Coupling between these lines and digital transitions on the backend could potentially feedback into the analog sections of the chip. This risk can be reduced by providing shield metal layers to isolate the analogue buses over the digital section. The risk is further mitigated by the incorporation of bypass capacitance throughout and within the pipeline layout.

A concern of the task force is that these two versions begin a process where the final chip really does come in two versions. If the DØ version of the chip shows no significant degradation in analog performance for CDF, then an exactly common chip could be used by both experiments.

A concern of the task force is that the Sept 2001 schedule for the first full size chip potentially limits the choice of available options. This concern arises because there may or may not be sufficient testing time of the FNAL test chip because integration must begin well ahead of the actual submission date. The adherence to the Sept 2001 schedule also has lead to initial pad frame layouts that are more complex than required in that duplicate pads are used where single pads with additional logic would suffice.

Recommendations:

- CDF and DØ are recommended to seek an exactly common chip with very high priority for the reasons cited above unless it is absolutely technically necessary to have two distinct chips. The laboratory should endorse this effort.
- The padframe layout and the power busing should be finalized as quickly as possible
- Clear sets of criteria should be given for acceptance of the various designs
- Having a well performing first, completely functional chip should be the highest priority
- The task force supports the review committee's recommendation for test chip evaluation before full chip submission
- Test submissions should be followed with a full verification of the design simulation, with changes if necessary, followed by an external review before final submission for production.

Resources

One thing the projects definitely have in common is the use of resources at SiDet. These resources are at this moment insufficient. There is an immediate need for two CMM operators and SiDet anticipates the need to hire (or internally transfer) 8 technicians. In addition, two more mechanical engineers should be identified to work on the Run2b silicon projects. R&D work for the support structures should start immediately and resources should be made available. These items have a long lead time and adequate contingency can be provided by starting now. More details on SiDet resources can be found in the cost and schedule review.

Summary

The creation of the task force has resulted in fruitful, interesting discussions on many aspects of the projects and has led to a better understanding of the similarities and differences between the CDF and DØ proposals. The designs of the Run 2b detectors are evolving and it is possible that even more similarities will be uncovered which can be pursued. Although the details are necessarily different, due to external constraints, the

choice of the same materials and technologies can result in great benefits in R&D time, production time and costs. A lot of work remains to be done to reap these benefits. To this end, it is strongly recommended that the discussions between the projects continue on a regular basis in a well defined forum. It is suggested that SiDet provides this forum through regular meetings. Common procurement contracts should be instigated whenever possible and common R&D efforts should be given resources and engineering support.

The SVX4 chip design has made good progress and is on-track to provide one common chip for both projects. Both experiments should give highest priority to having a common chip. It is recommended that before submission for production a full verification of the design simulations and an independent external review is carried out.